Attorney Docket No.: SP-5106 US
First Inventor: Sharada Yeluri
Title: Forwarding Load Data To Younger Instructions In Annex

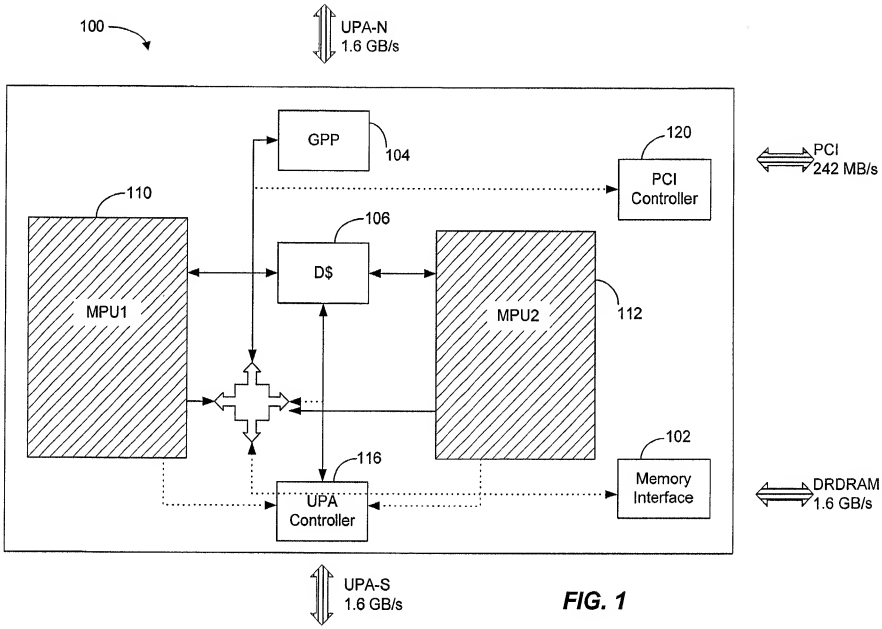

FIG. 1

100
MPU1
110
PC1
Instruction Cache
210
Instruction Aligner
212
Instruction Buffer
214
PCU
226
MFU3
MFU2
MFU1
GFU
220
222
Register Files
216
224
Load/Store Unit
218
MPU2
112
PC2
Shared Data Cache and Synchronization Area
106

FIG. 2

FIG. 3

20220-Shortbot

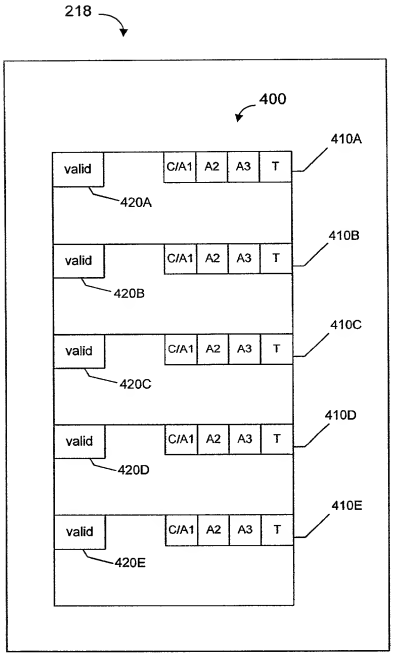
218
400
410A
valid
C/A1
A2
A3
T
420A
410B
valid
C/A1
A2
A3
T
420B
410C
valid
C/A1
A2
A3
T
420C
410D
valid
C/A1
A2
A3
T
420D
410E
valid
C/A1
A2
A3
T
420E

FIG. 4

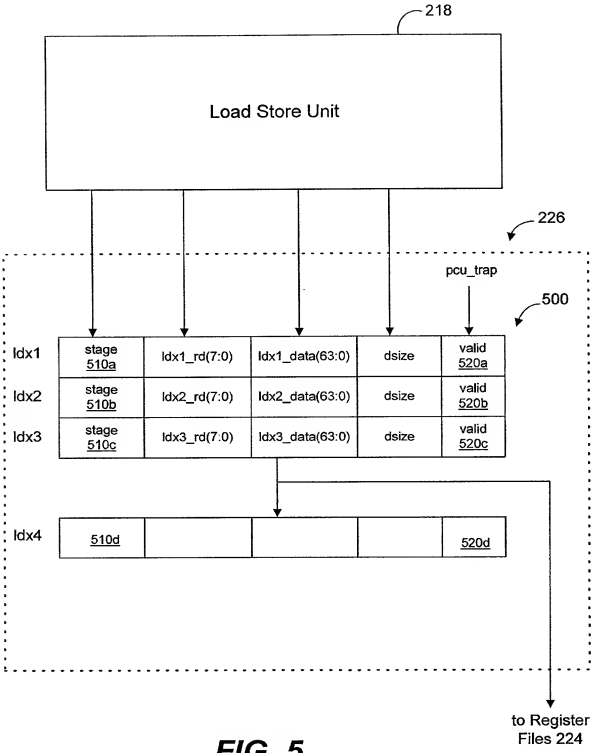
218
Load Store Unit
226
pcu_trap
500
ldx1
stage 510a
ldx1_rd(7:0)
ldx1_data(63:0)
dsize
valid 520a
ldx2
stage 510b
ldx2_rd(7:0)
ldx2_data(63:0)
dsize
valid 520b
ldx3
stage 510c
ldx3_rd(7:0)
ldx3_data(63:0)
dsize
valid 520c
ldx4
510d
520d
to Register Files 224

FIG. 5

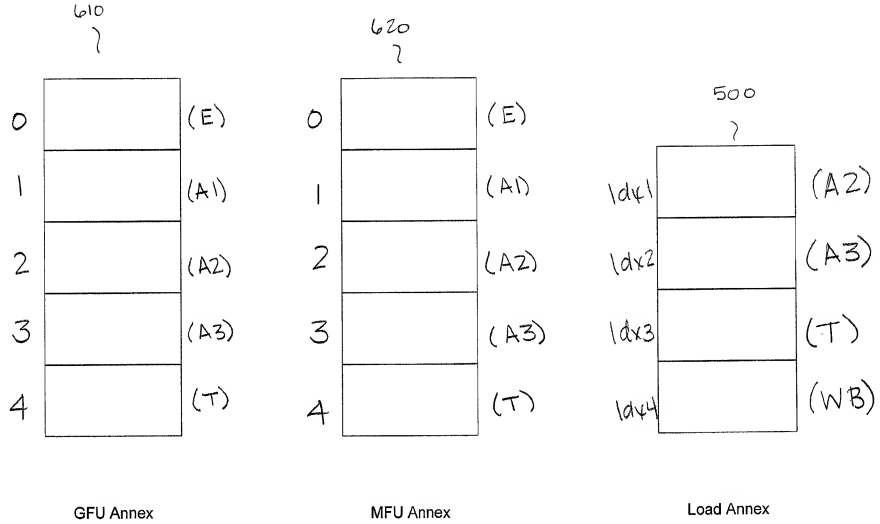
610
0
1
2
3
4
(E)
(A1)
(A2)
(A3)
(T)
GFU Annex
620
0
1
2
3
4
(E)
(A1)
(A2)
(A3)
(T)
MFU Annex
500
Idx1
Idx2
Idx3
Idx4
(A2)
(A3)
(T)
(WB)
Load Annex

FIG. 6

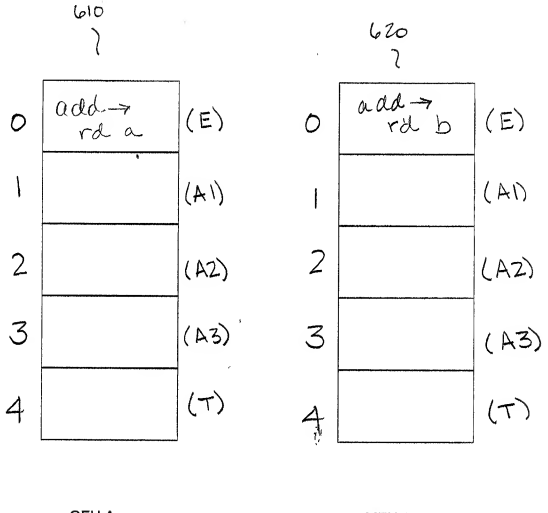

FIG. 6/7

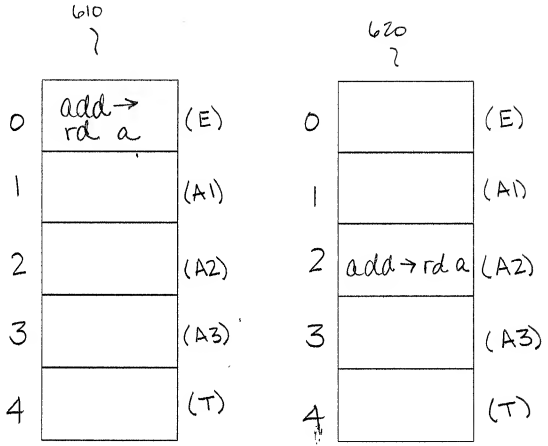

FIG. 8

cycle	1	2	3	4	5	6	7	8	9	10	11	12
(1)	D	E	C/A1	A2 (1dx1)	A3 (1dx2)	T1 (1dx3)	WB (1dx4)					
(2)		D	D	D	E	A1	A2	A3	T	WB		
(3)					D	E	A1	A2	A3	T	WB	
(4)						D	E	A1	A2	A3	T	WB
(5)							D					

Fig. 9

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Cycle 4

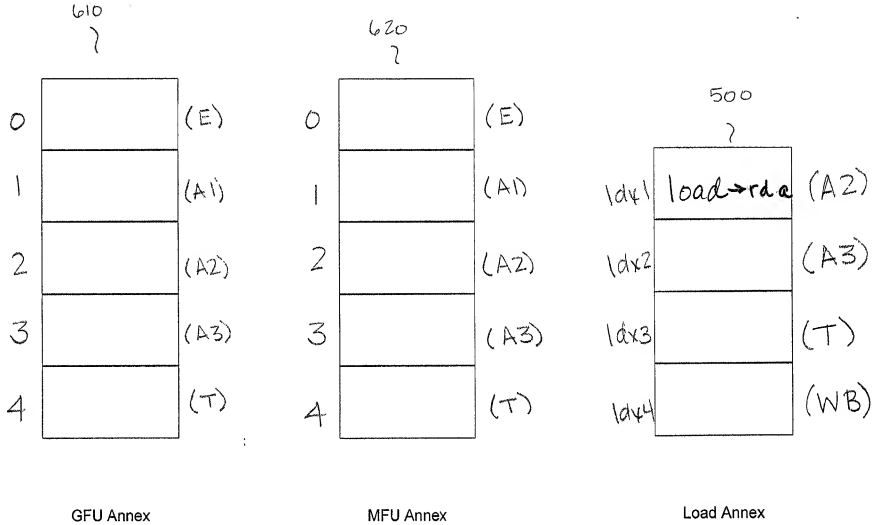

FIG. 6 10

Cycle 5

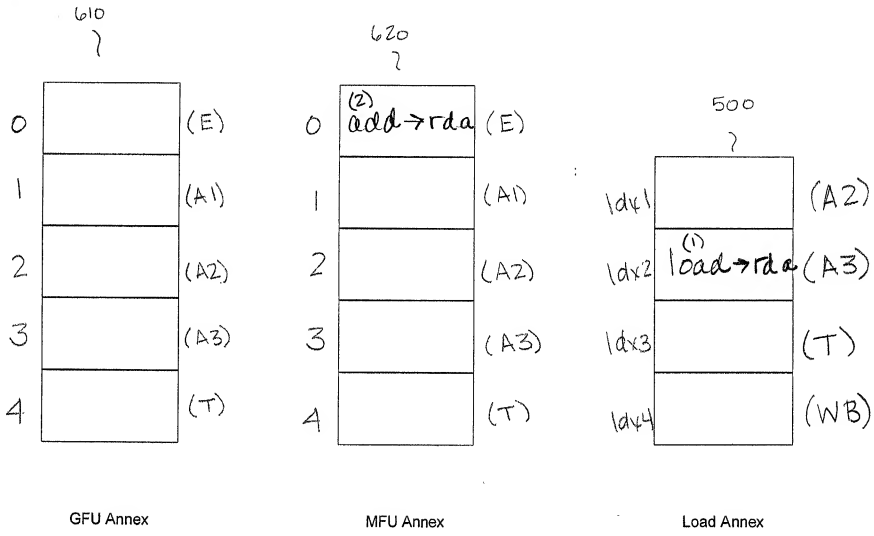

FIG. 6 11

Cycle 6

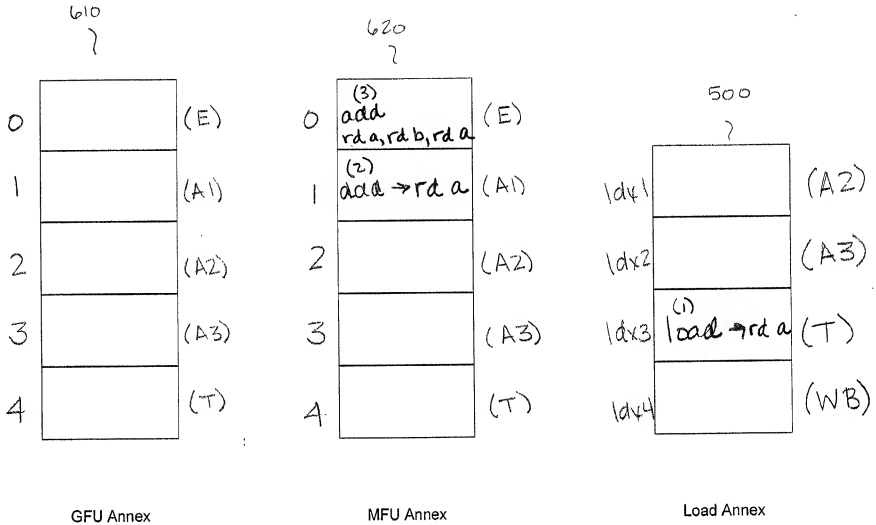

FIG. 6 12

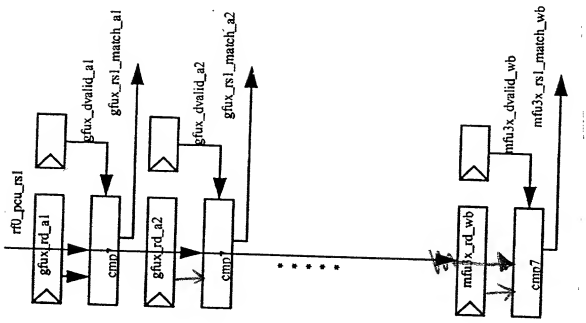
rf0_pcu_rs1
gfux_rd_a1
gfux_dvalid_a1
gfux_rs1_match_a1
cmp1
gfux_rd_a2
gfux_dvalid_a2
gfux_rs1_match_a2
cmp1
mfui3x_rd_wb
mfui3x_dvalid_wb
mfui3x_rs1_match_wb
cmp7

Fig. 13